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Sun

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(54) **METHODS OF FABRICATING AN F-RAM**

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(51) **Int. Cl.**

H01L 21/00	(2006.01)
H01L 49/02	(2006.01)
H01L 27/115	(2006.01)

(52) **U.S. Cl.**
CPC ***H01L 28/56*** (2013.01); ***H01L 27/11507*** (2013.01)

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CPC G06F 11/3037; G06F 11/008; G06F 11/3058; G06F 11/004; G06F 11/0703; G06F 11/1008; G06F 11/1666; G06F 11/167; G06F 11/183; G06F 11/20; G06F 11/3055; G06F 11/34; G06F 11/3409; G06F 11/3433; H01L 2924/00; H01L 2924/0002; H01L 2924/00014; H01L 23/53238; H01L 21/76843; H01L 21/76834; H01L 21/76846; H01L 21/76849; H01L 21/76867; H01L 2224/05686; H01L 23/53295; H01L 2924/12042
USPC 711/103, 163, 146, 105, 119, 130, 133, 711/149, 170, 3; 257/532, 295, 300, 316, 5, 257/506, 788, 792; 438/3, 241, 381, 127, 438/386, 387, 763
See application file for complete search history.

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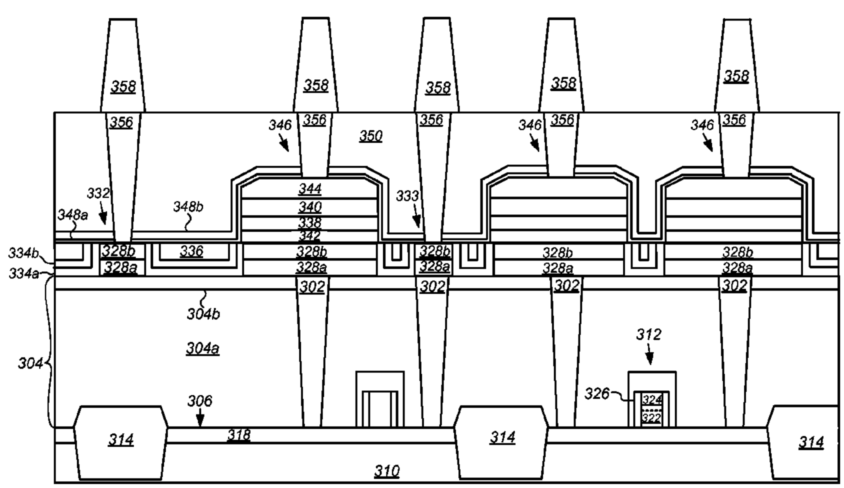
Primary Examiner — Robert Bachner

(57) **ABSTRACT**

Methods of forming F-RAM cells are described. The method includes forming a contact extending through a first dielectric layer on a surface of a substrate. A barrier structure is formed over the contact by depositing and patterning a barrier layer. A second dielectric layer is deposited over the patterned barrier layer and planarized to expose a top surface of the barrier structure. A ferro-stack is deposited and patterned over the barrier structure to form a ferroelectric capacitor. A bottom electrode of the ferroelectric capacitor is electrically coupled to the diffusion region of the MOS transistor through the barrier structure. The barrier layer is conductive so that a bottom electrode of the ferroelectric capacitor is electrically coupled to the contact through the barrier structure. In one embodiment, patterning barrier layer comprises concurrently forming a local interconnect (LI) on a top surface of the first dielectric layer.

20 Claims, 17 Drawing Sheets



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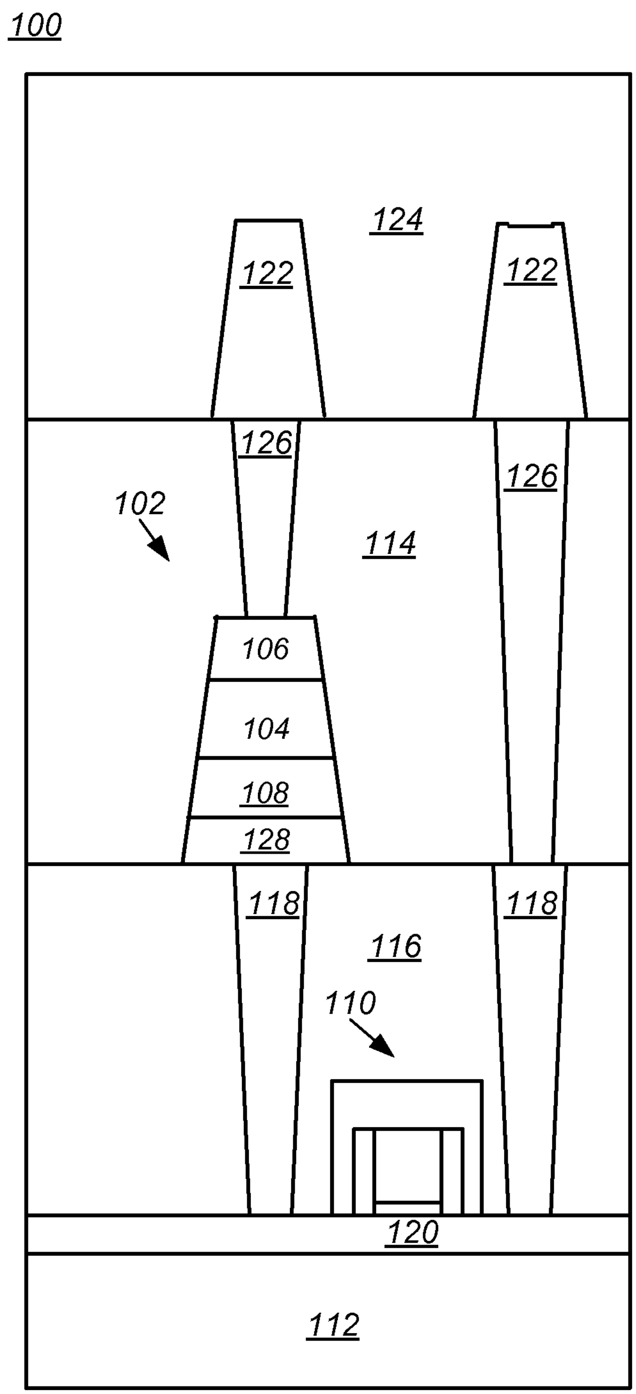


FIG. 1
(PRIOR ART)

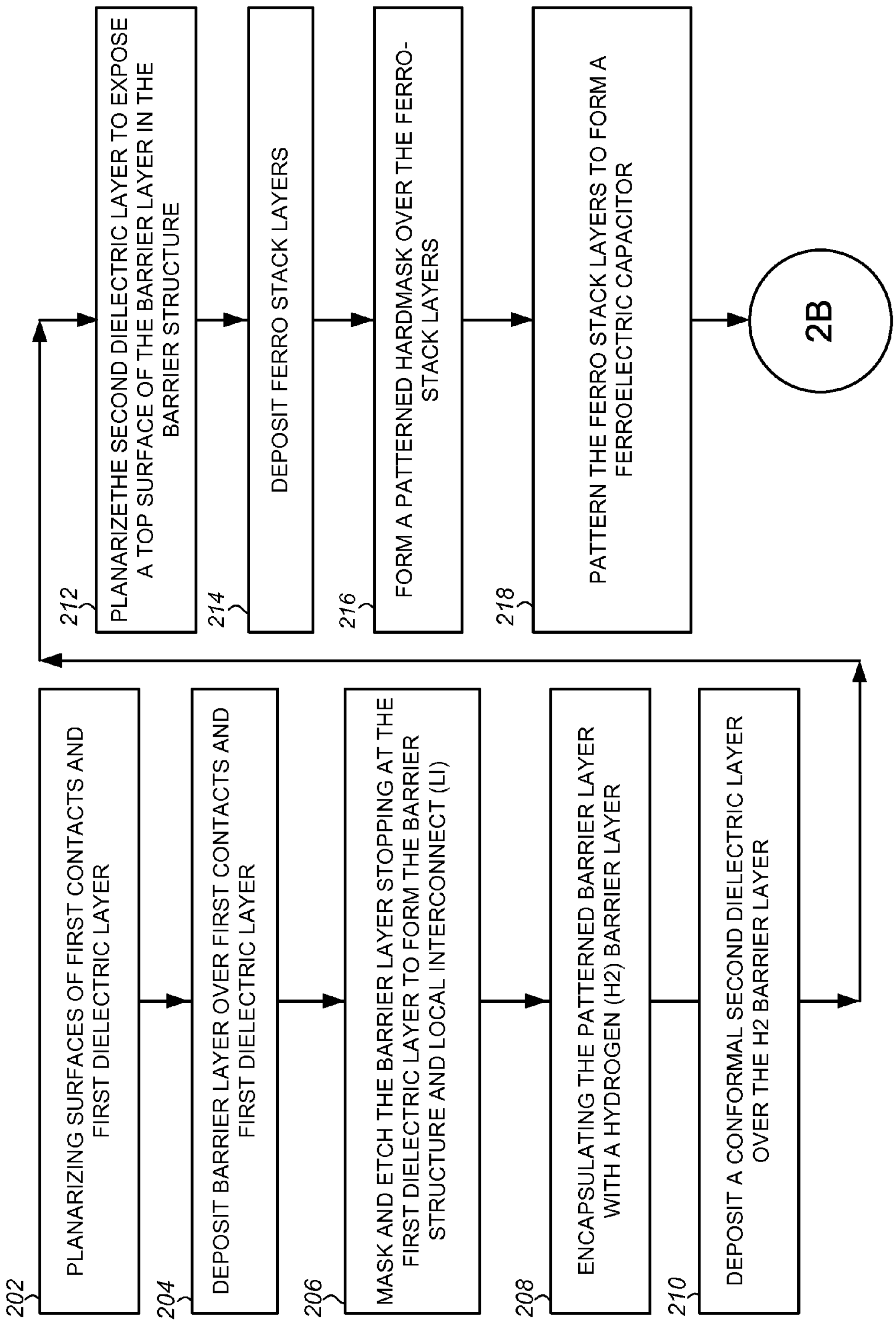

202
PLANARIZING SURFACES OF FIRST CONTACTS AND FIRST DIELECTRIC LAYER
204
DEPOSIT BARRIER LAYER OVER FIRST CONTACTS AND FIRST DIELECTRIC LAYER
206
MASK AND ETCH THE BARRIER LAYER STOPPING AT THE FIRST DIELECTRIC LAYER TO FORM THE BARRIER STRUCTURE AND LOCAL INTERCONNECT (LI)
208
ENCAPSULATING THE PATTERNED BARRIER LAYER WITH A HYDROGEN (H2) BARRIER LAYER
210
DEPOSIT A CONFORMAL SECOND DIELECTRIC LAYER OVER THE H2 BARRIER LAYER
212
PLANARIZETHE SECOND DIELECTRIC LAYER TO EXPOSE A TOP SURFACE OF THE BARRIER LAYER IN THE BARRIER STRUCTURE
214
DEPOSIT FERRO STACK LAYERS
216
FORM A PATTERNED HARDMASK OVER THE FERRO-STACK LAYERS
218
PATTERN THE FERRO STACK LAYERS TO FORM A FERROELECTRIC CAPACITOR
2B

FIG. 2A

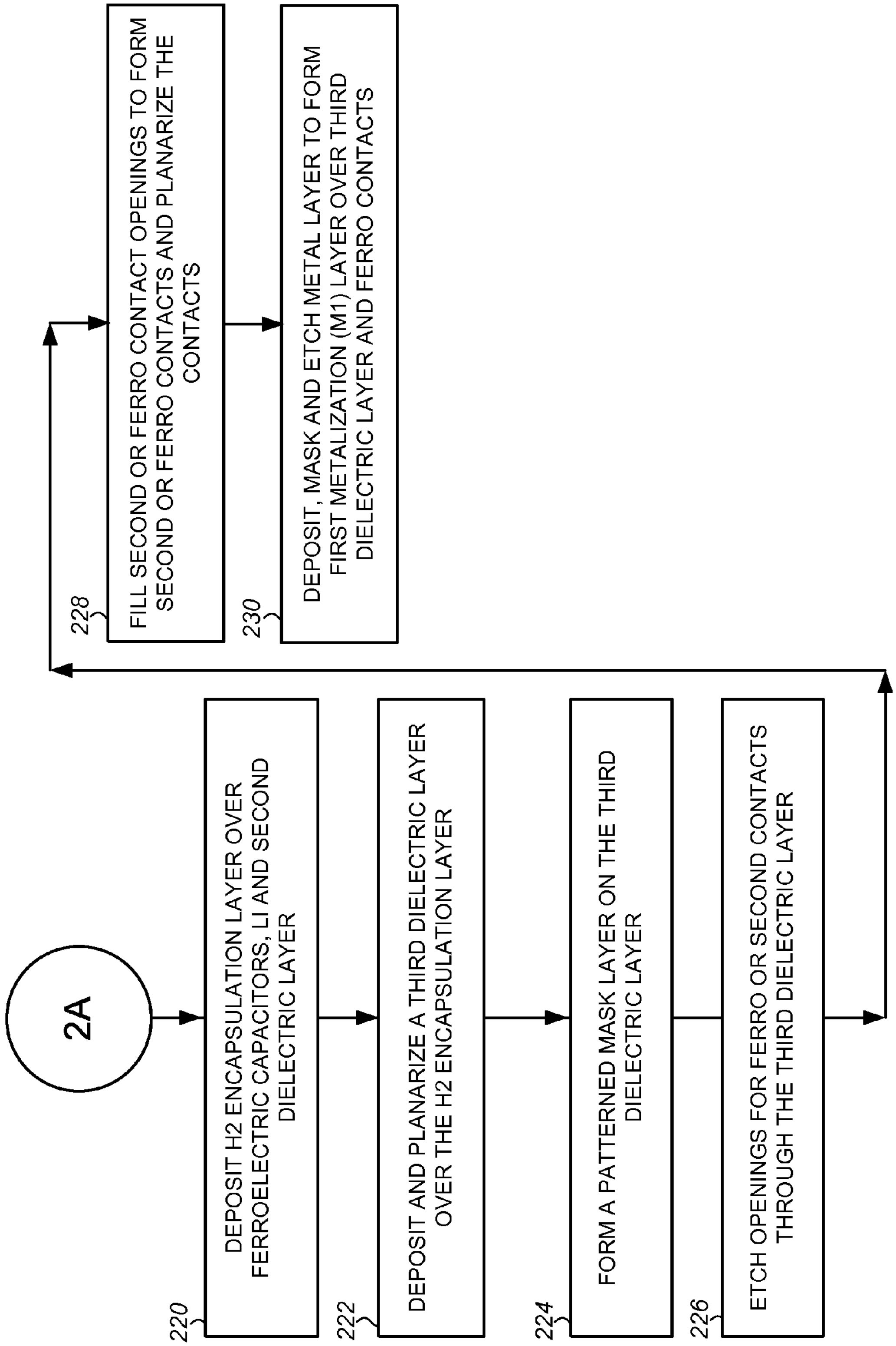
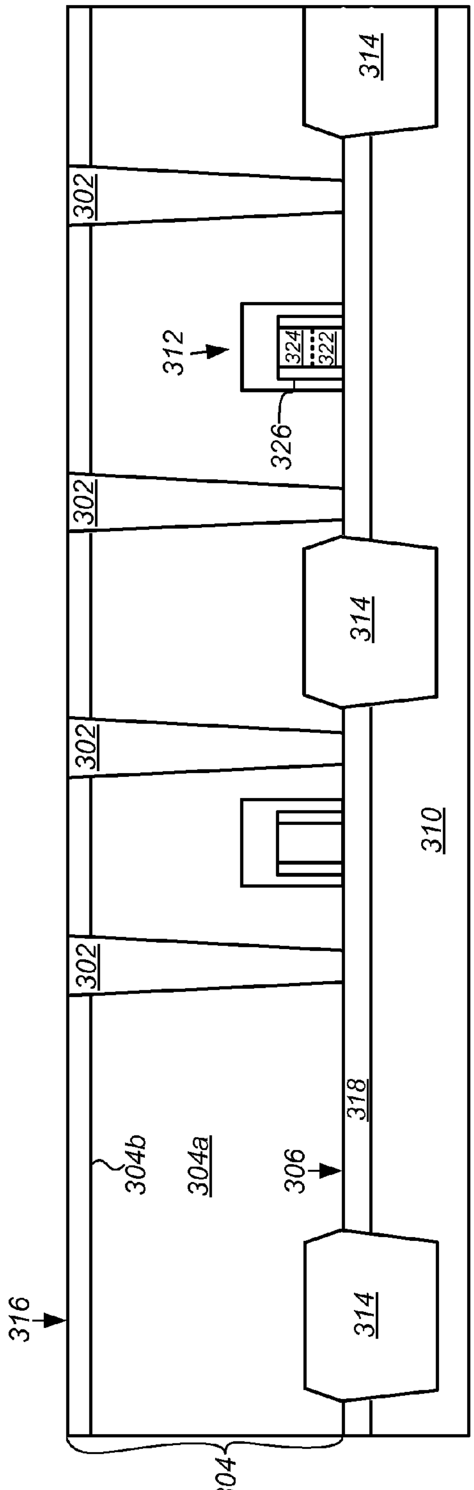

2A
220
DEPOSIT H2 ENCAPSULATION LAYER OVER FERROELECTRIC CAPACITORS, LI AND SECOND DIELECTRIC LAYER
222
DEPOSIT AND PLANARIZE A THIRD DIELECTRIC LAYER OVER THE H2 ENCAPSULATION LAYER
224
FORM A PATTERNED MASK LAYER ON THE THIRD DIELECTRIC LAYER
226
ETCH OPENINGS FOR FERRO OR SECOND CONTACTS THROUGH THE THIRD DIELECTRIC LAYER
228
FILL SECOND OR FERRO CONTACT OPENINGS TO FORM SECOND OR FERRO CONTACTS AND PLANARIZE THE CONTACTS
230
DEPOSIT, MASK AND ETCH METAL LAYER TO FORM FIRST METALIZATION (M1) LAYER OVER THIRD DIELECTRIC LAYER AND FERRO CONTACTS

FIG. 2B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302
302
318
304b
304a
306
310
316
314
304

FIG. 3A

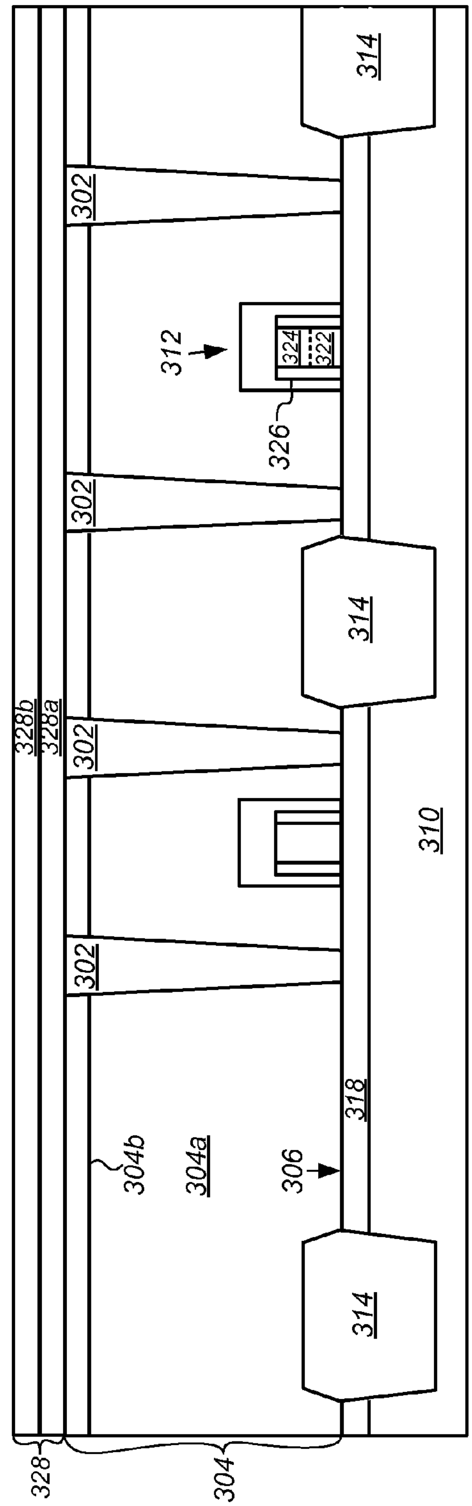
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FIG. 3B

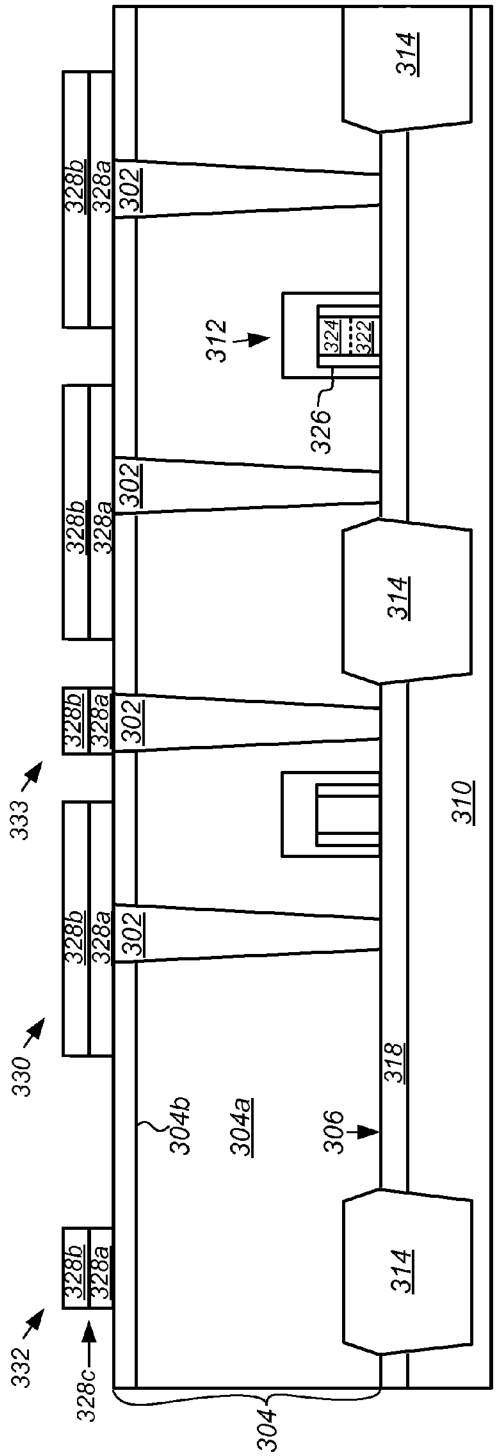
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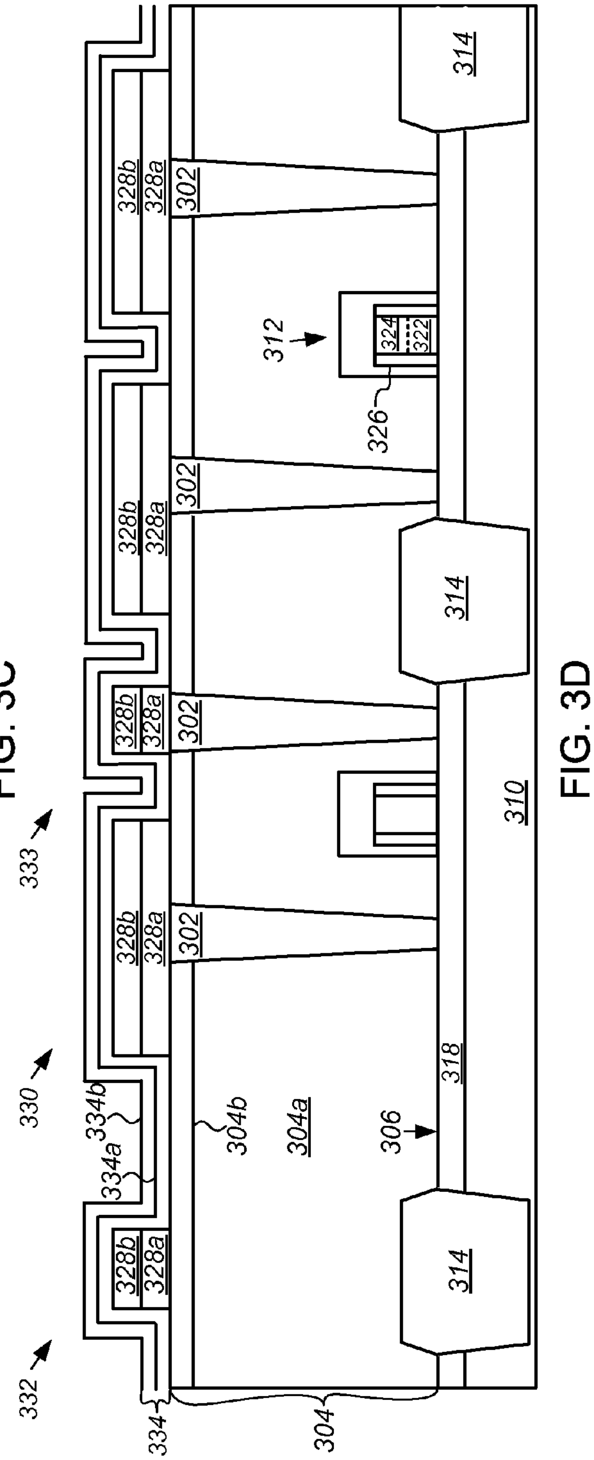
FIG. 3C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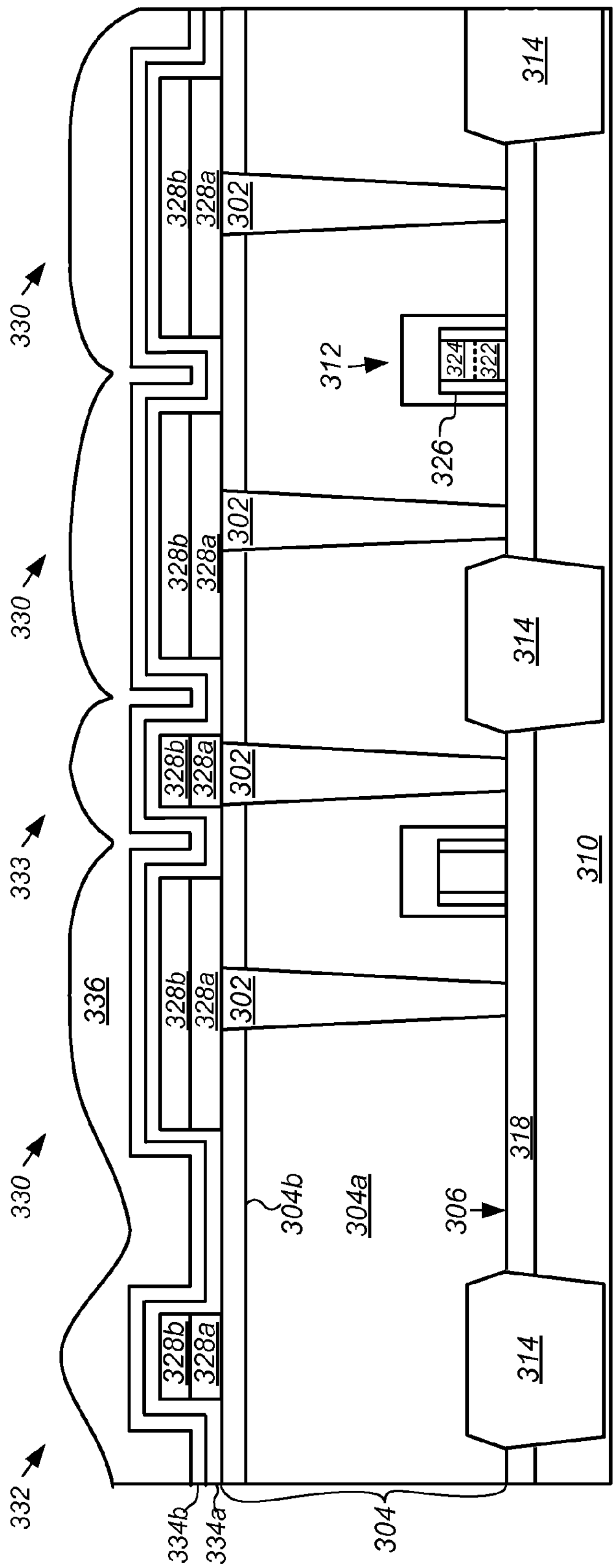
310
304

FIG. 3D



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334a
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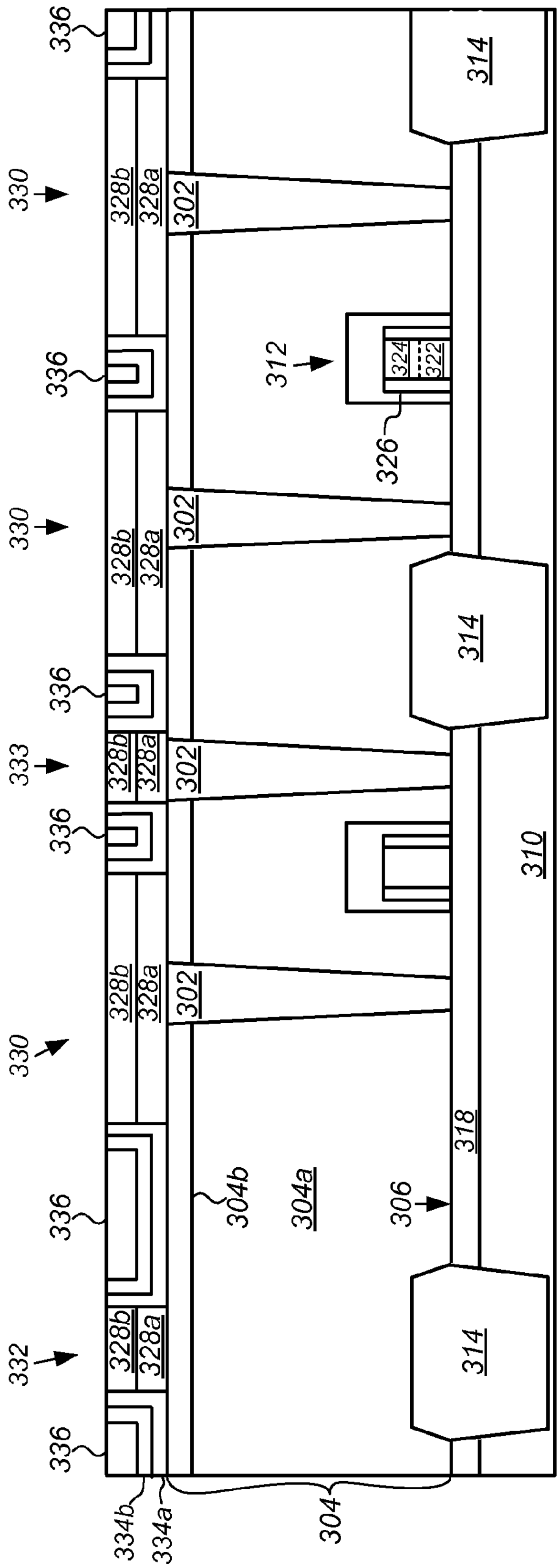
FIG. 3E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328b
328a
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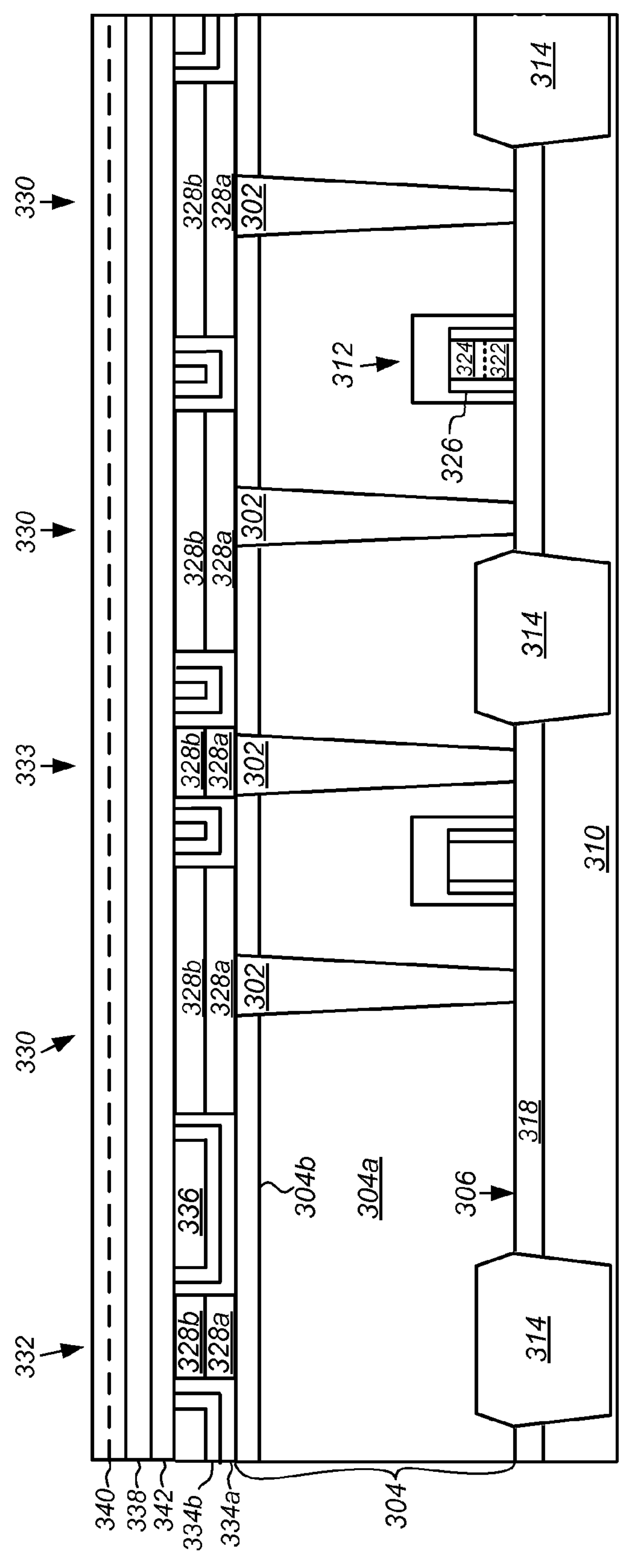
334b
334a
304

FIG. 3F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334b
334a
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FIG. 3G

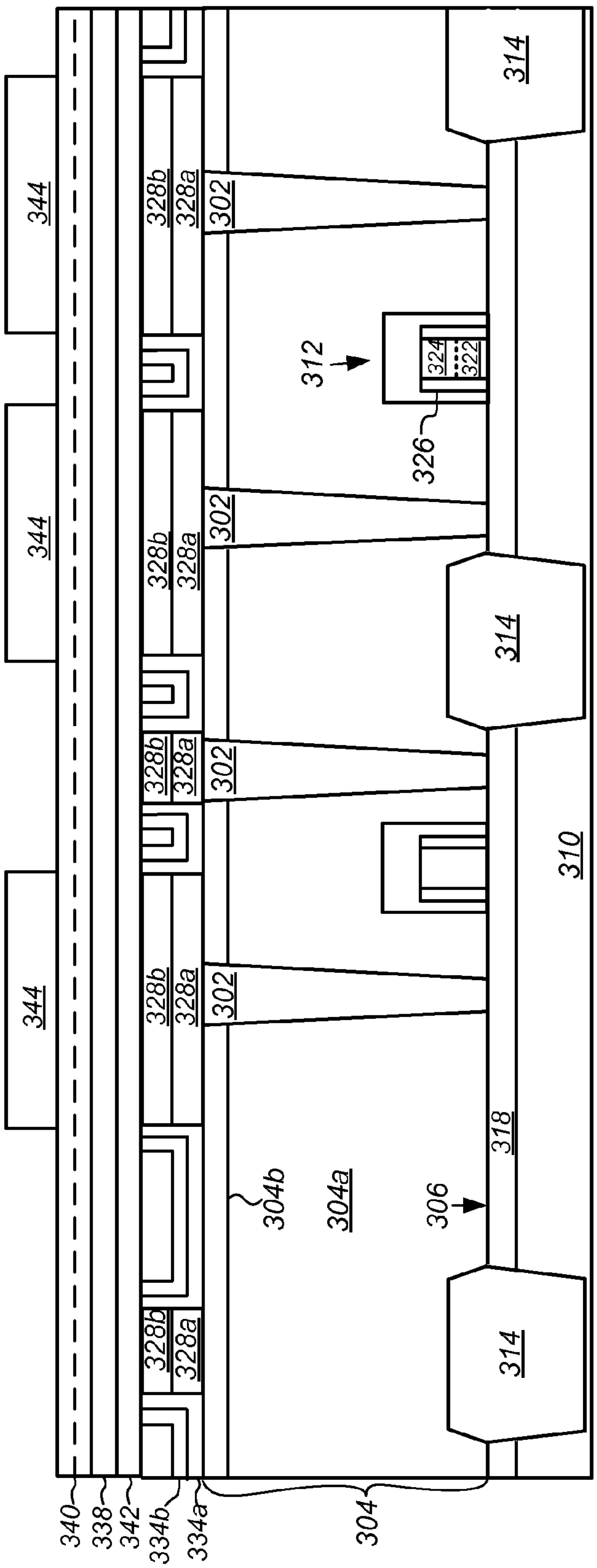
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FIG. 3H

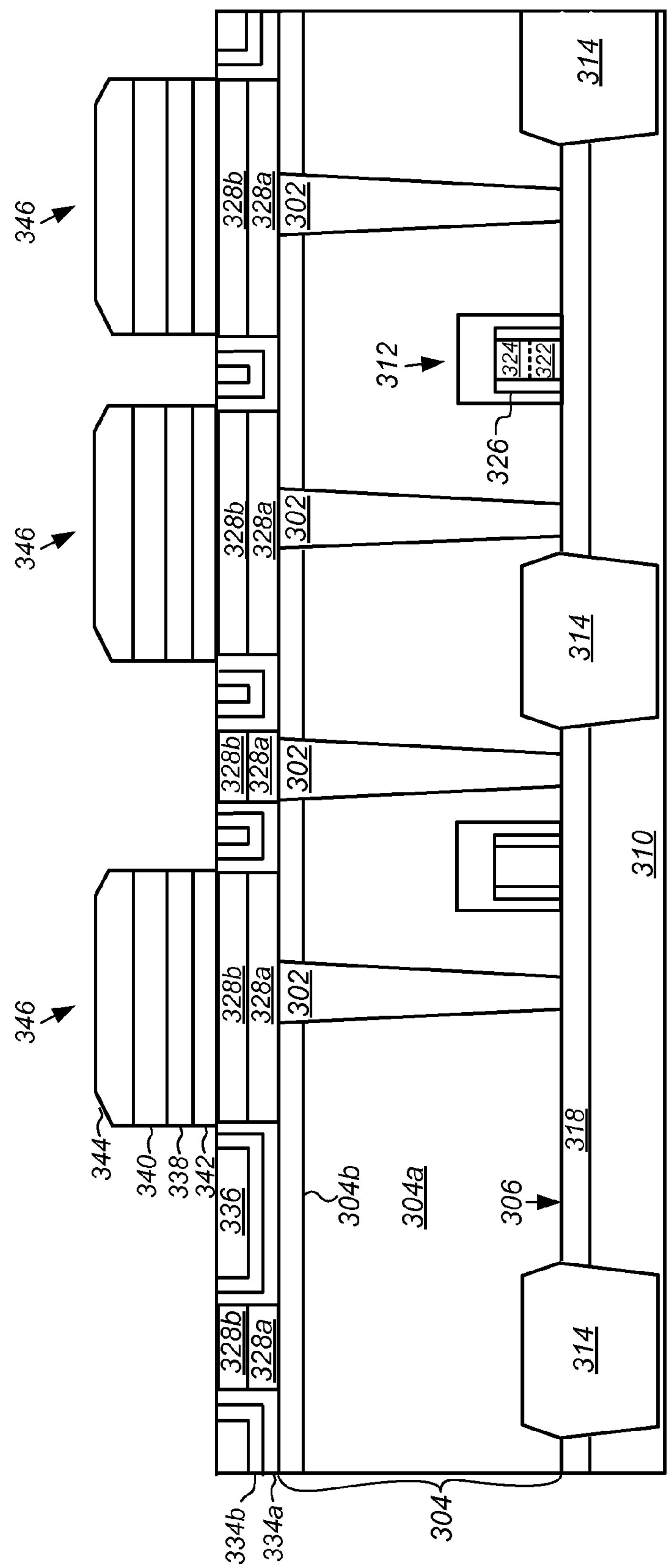
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FIG. 3I

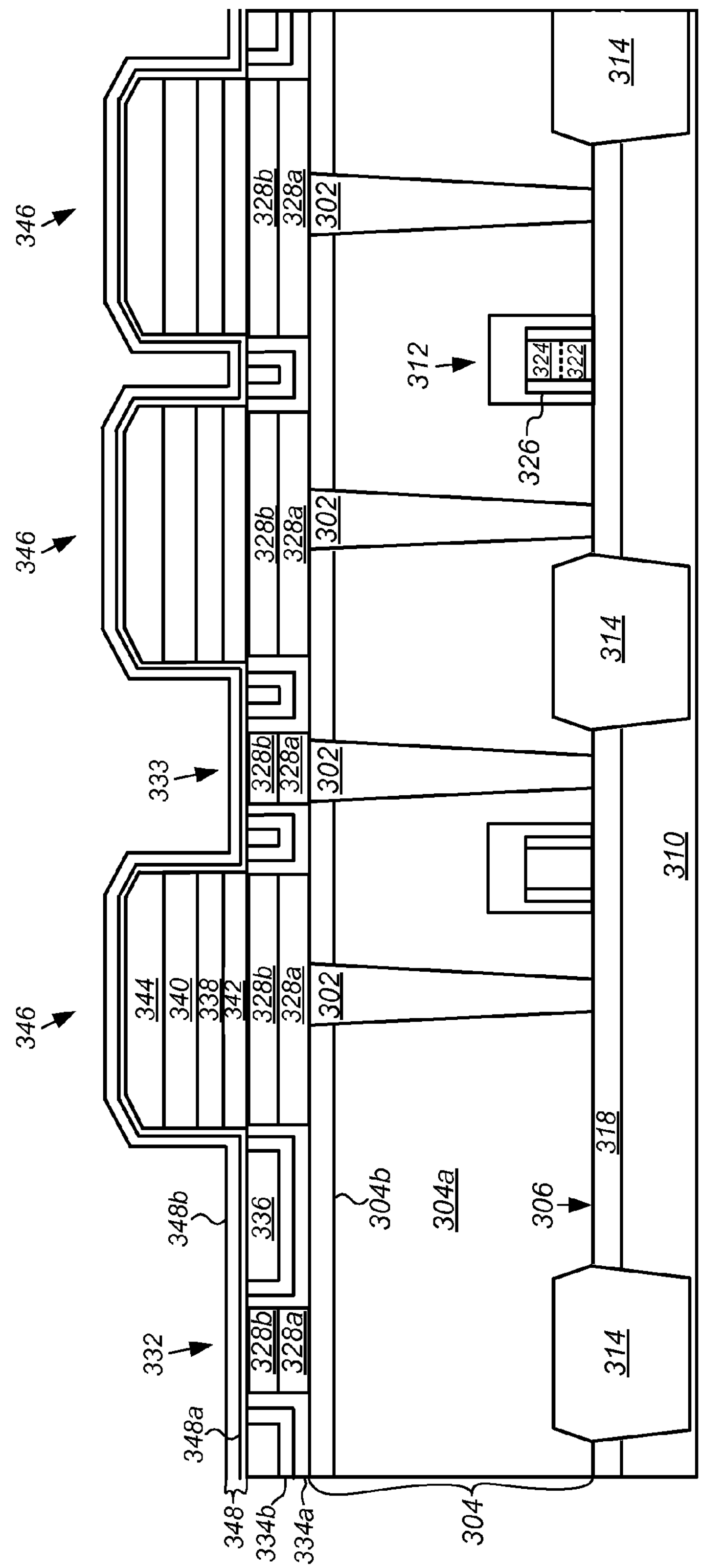
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FIG. 3J

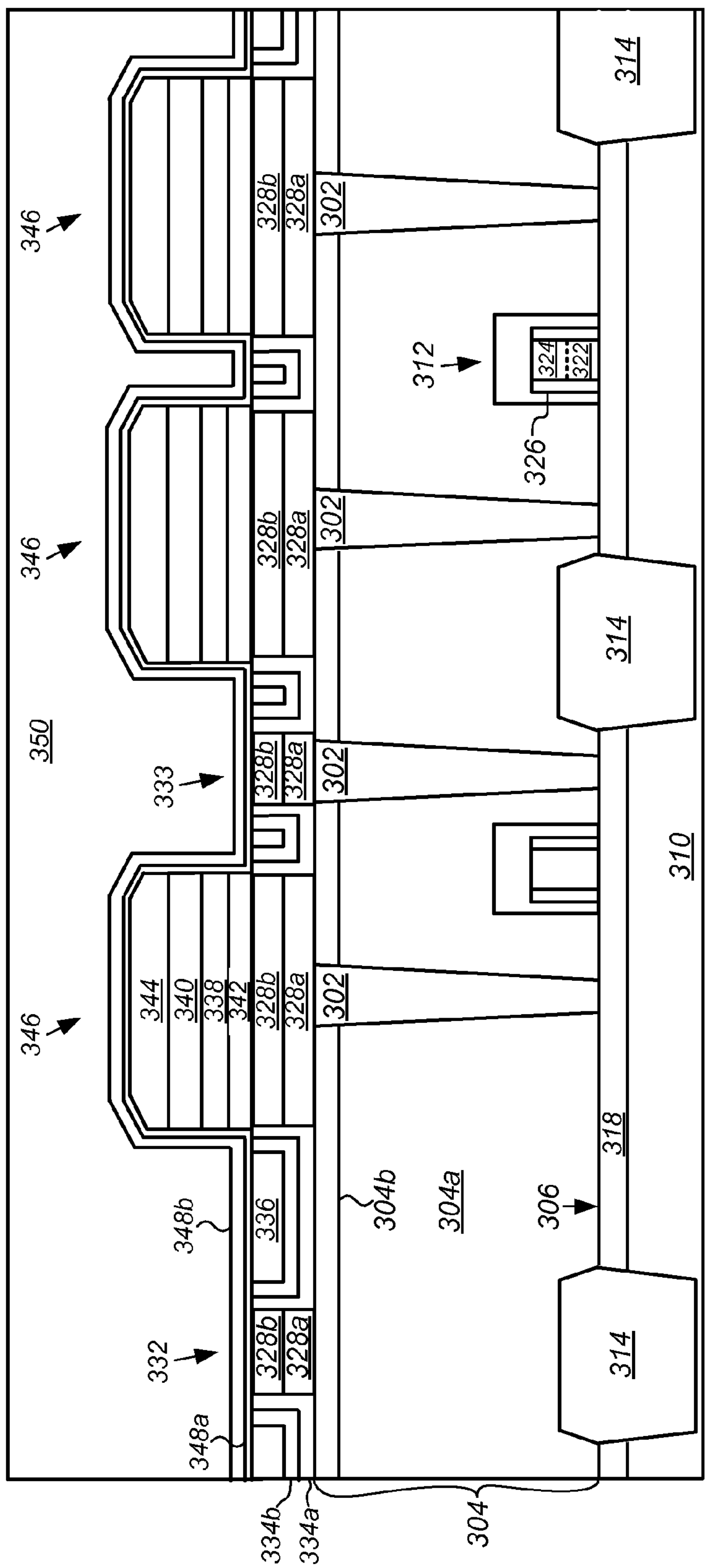
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FIG. 3K

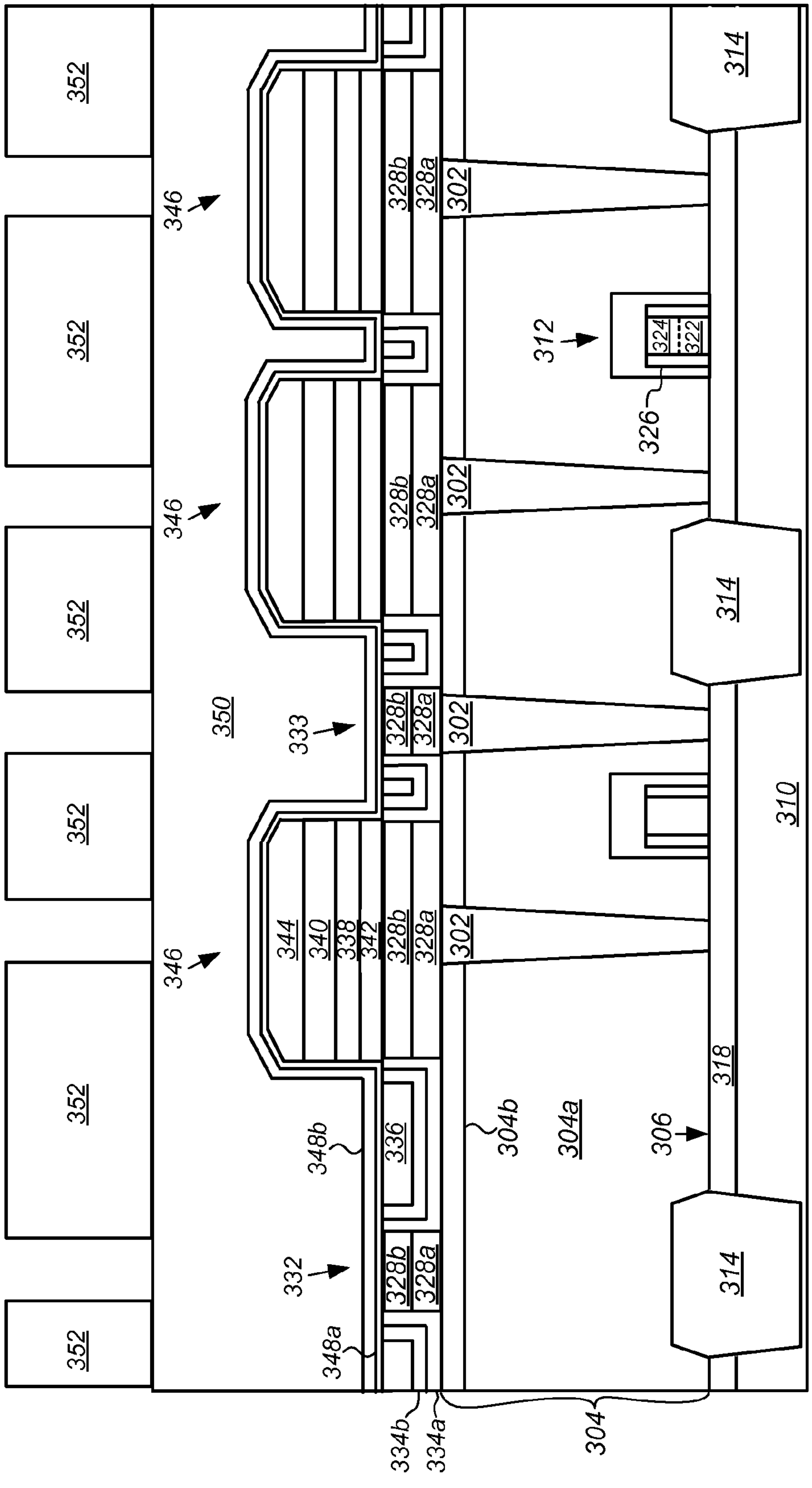
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FIG. 3L

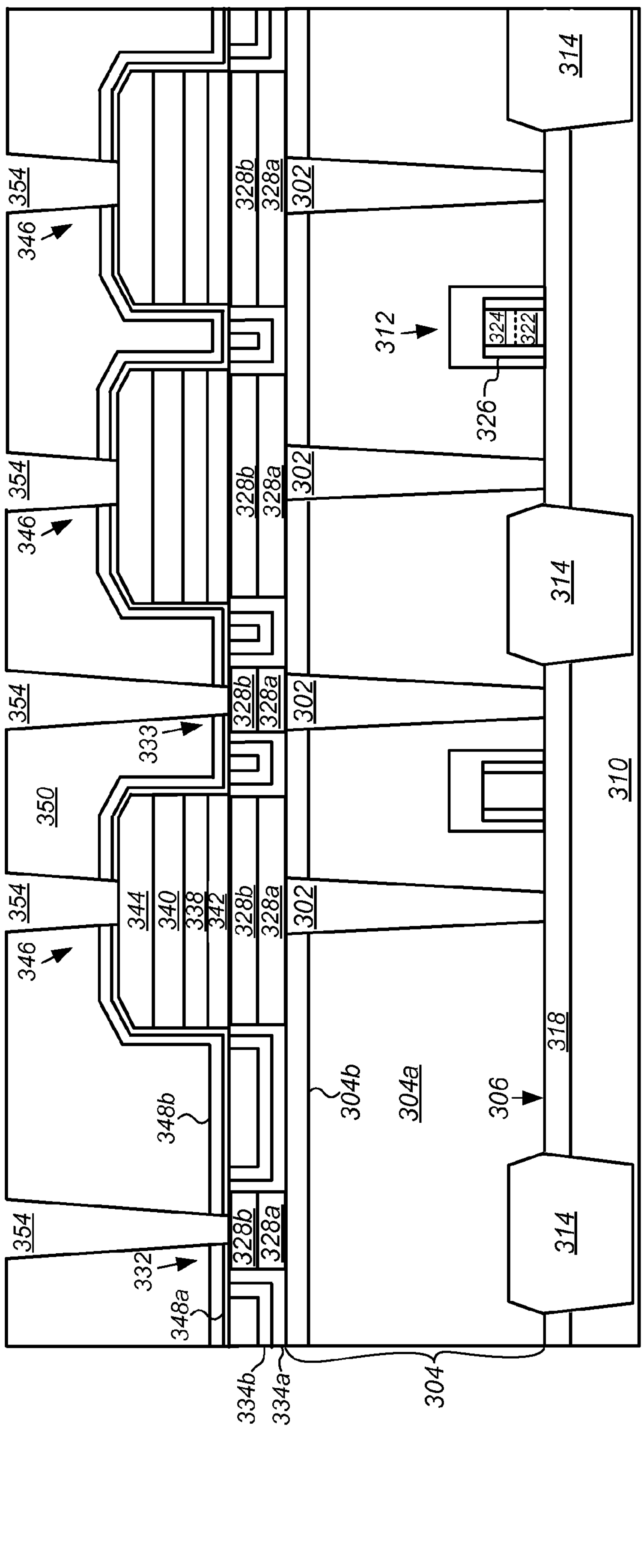
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FIG. 3M

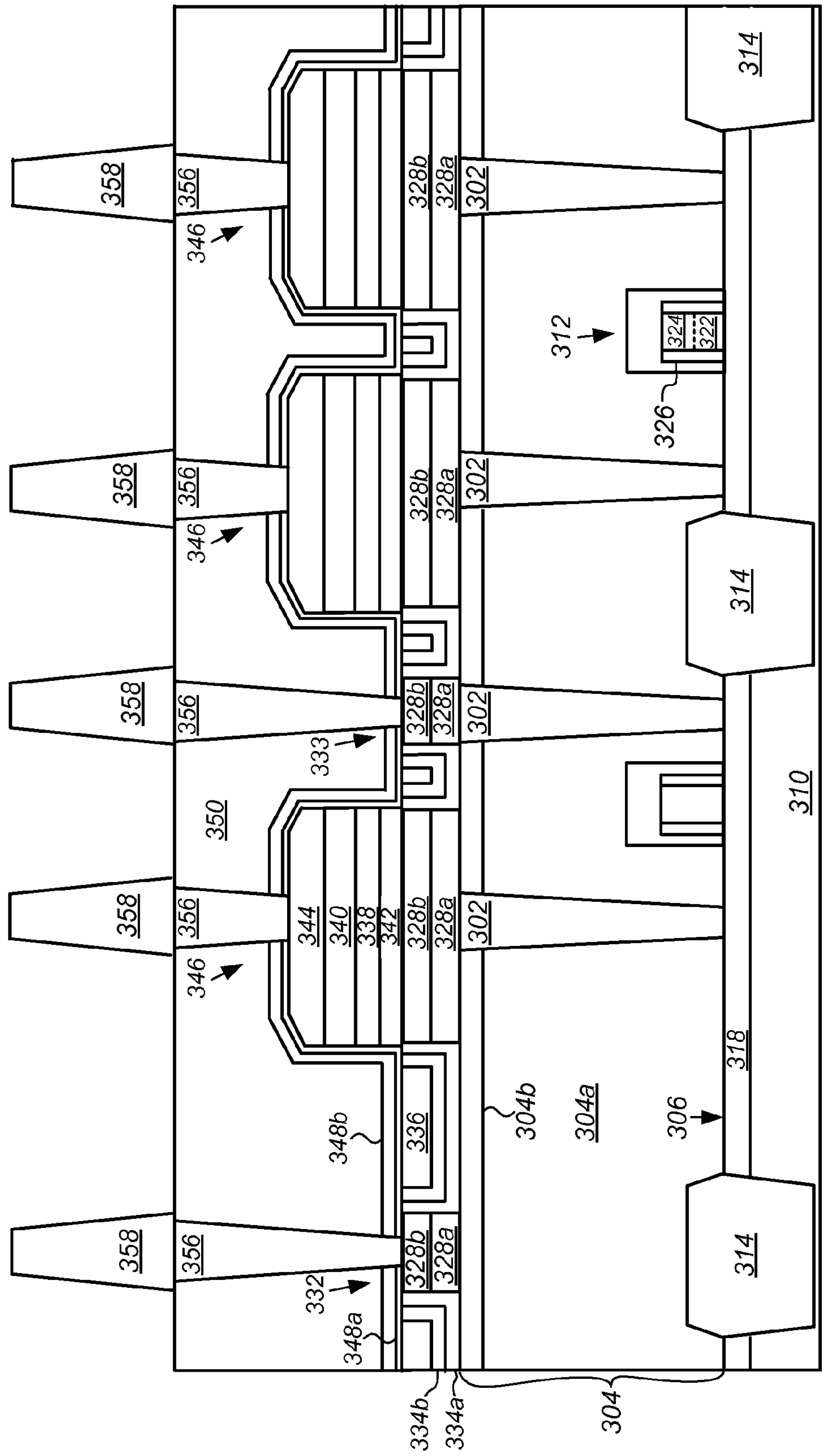
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FIG. 3N

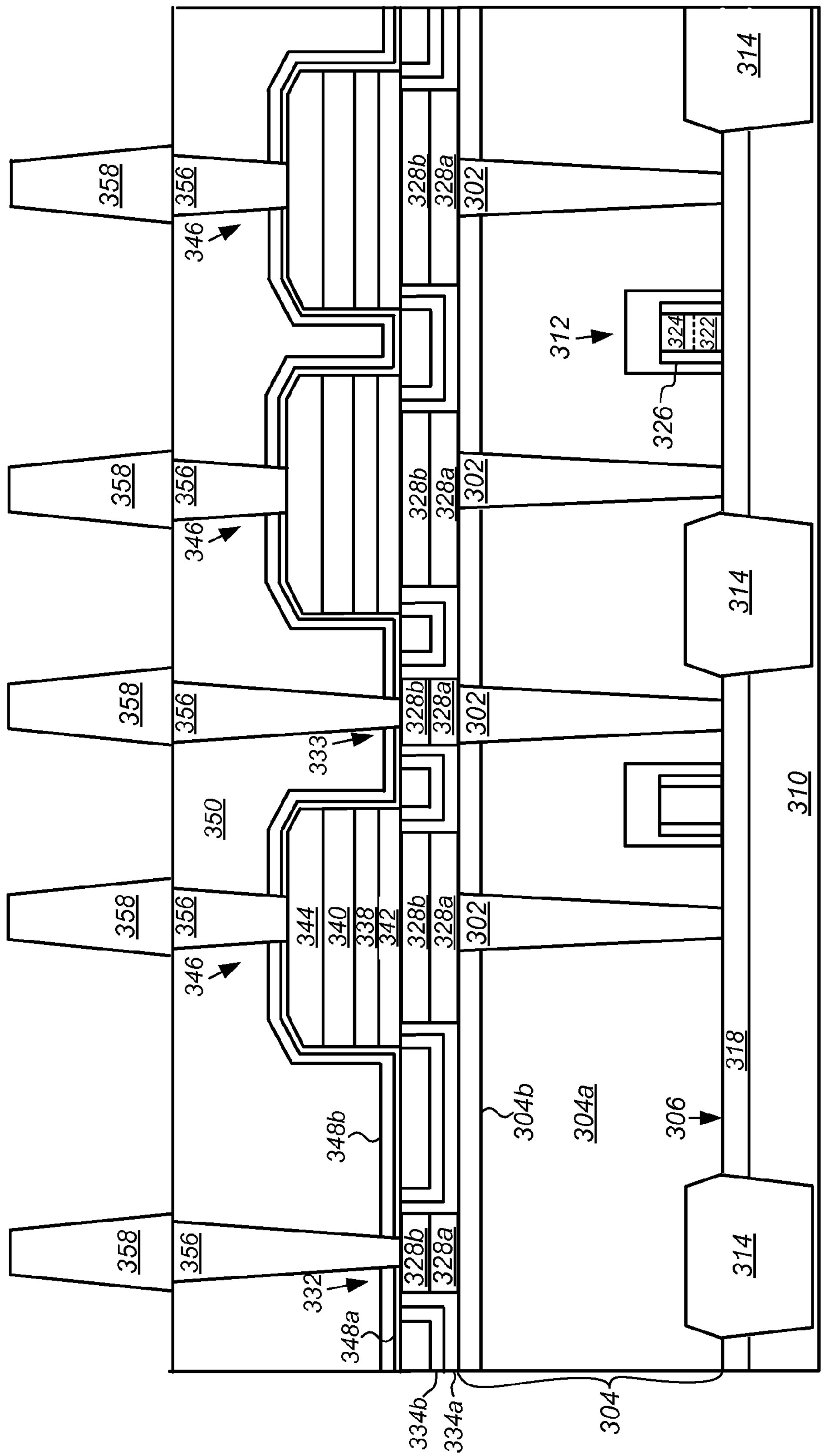
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FIG. 4

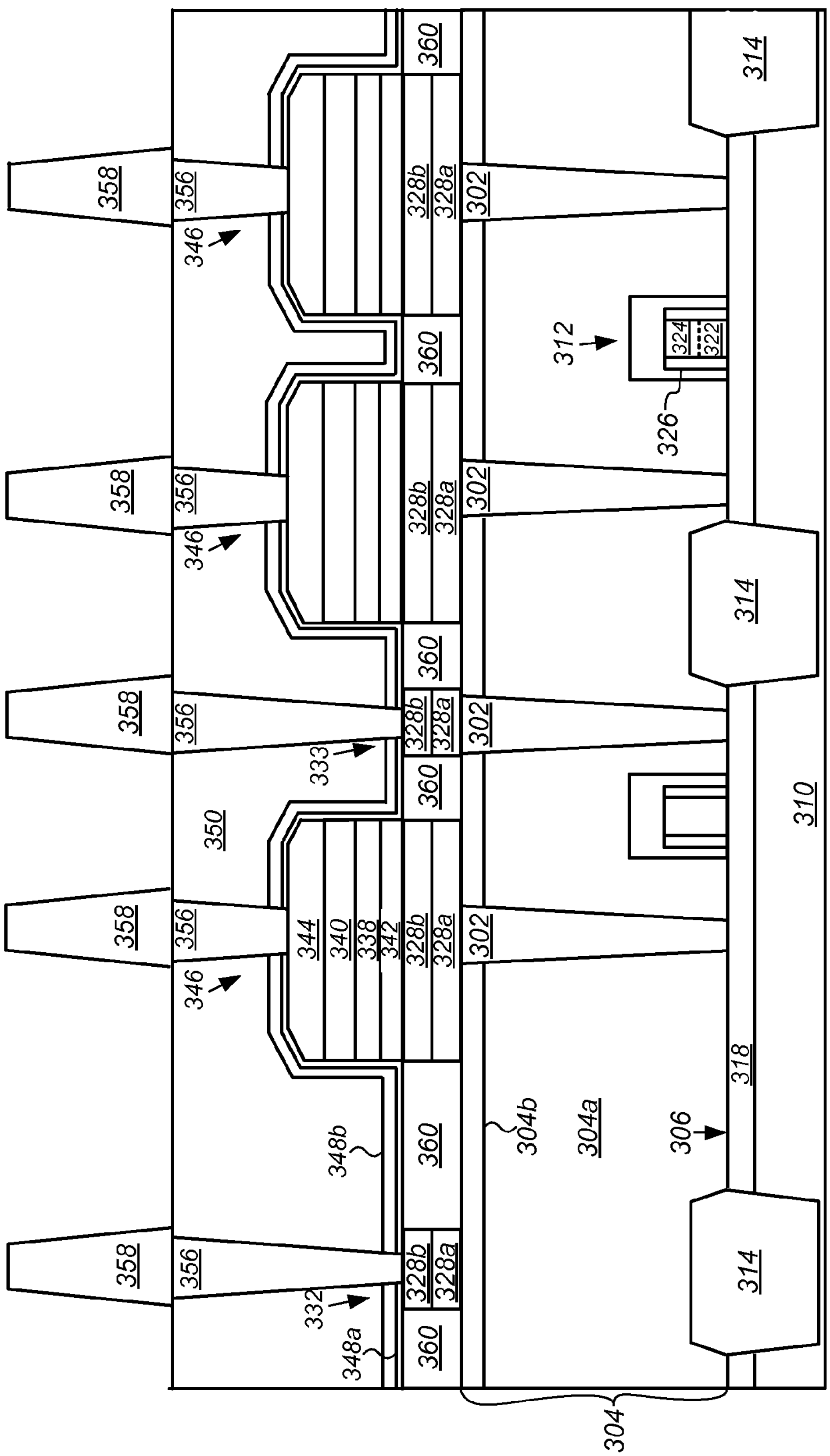
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FIG. 5

METHODS OF FABRICATING AN F-RAM

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of priority under 35 U.S.C. 119(e) to U.S. Provisional Patent Application Ser. No. 62/169,042, filed Jun. 1, 2015, which is incorporated by reference herein in its entirety.

TECHNICAL FIELD

The present disclosure relates generally to semiconductor devices, and more particularly to ferroelectric random access memories (F-RAM) including embedded or integrally formed ferroelectric capacitors and complementary metal-oxide-semiconductor (CMOS) transistors and methods for fabricating the same.

BACKGROUND

Ferroelectric random-access memories (F-RAM) typically include a grid or an array of storage elements or cells, each including at least one ferroelectric capacitor and one or more associated transistors to select the cell and control reading or writing thereto.

When an external electric field is applied across a ferroelectric material of a ferroelectric capacitor in the cell, dipoles in the material align with the field direction. After the electric field is removed, the dipoles retain their polarization state. Data is stored in the cells as one of two possible electric polarizations in each data storage cell. For example, in a one transistor-one capacitor (1T1C) cell, a "1" may be encoded using a negative remnant polarization, and a "0" is encoded using a positive remnant polarization.

FIG. **1** illustrates a cross-sectional view of a portion of a F-RAM cell **100** fabricated according to a conventional method. Referring to FIG. **1**, the ferroelectric capacitor **102** in an F-RAM cell typically includes a ferroelectric material **104** between an upper electrode **106** and a lower electrode **108**. Transistors **110** in the cell **100** are typically metal-oxide-semiconductor (MOS) transistors fabricated on a substrate **112** using a standard or baseline complimentary-metal-oxide-semiconductor (CMOS) process flows, involving the formation and patterning of conducting, semiconducting, dielectric and materials. The composition of these materials, as well as the composition and concentration of processing reagents, and temperature used in such a CMOS process flow are stringently controlled for each operation to ensure the resultant MOS transistors will function properly. Thus, in conventional methods of fabricating F-RAM the ferroelectric capacitor **102** is fabricated in a separate F-RAM layer **114** overlying a CMOS layer **116** in which the MOS transistors **110** are fabricated and connected thereto by one or more contacts **118** extending to a diffusion region **120** of the MOS transistor in the substrate **112** and/or by a separate wiring layer **122** fabricated in yet another dielectric layer **124** overlying the F-RAM layer **112** and connected to the MOS transistors and ferroelectric capacitor through additional contacts **126**.

Materials and processes typically used to fabricate the CMOS transistors **110**, contacts **118** and wiring layer **122** are incompatible with ferroelectric capacitor process flow, and can detrimentally impact their performance. In particular, when fabricating the ferroelectric capacitor **102** over a contact **118** in the CMOS layer **116** processes used to fabricate the ferroelectric capacitor can oxidize a metal used in the contact. Thus, ferroelectric capacitors **102** formed over such contacts **118** typically must include an oxygen barrier **128** between the contact and bottom electrode.

It will be understood by those skilled in the art that the above described conventional method of fabricating F-RAM undesirably increases an aspect ratio of the ferroelectric capacitors **102**, as well as the overall size or height of the F-RAM cell **100**, and require several extra mask and processing steps, all of which increase fabrication time, costs, and defect density lowering a yield of working memories.

SUMMARY

Non-volatile memory cells including complimentary metal-oxide-semiconductor (CMOS) transistors and embedded ferroelectric capacitors formed according to methods of the present disclosure minimizes changes to the CMOS process flow, reducing cost of fabricating ferroelectric random access memories (F-RAM), lowering defect density and enabling tighter design rules.

In one embodiment, the method includes forming a contact extending through a first dielectric layer on a surface of a substrate. A barrier structure is formed over the contact. Generally, forming the barrier structure includes: (i) depositing a barrier layer over a top surface of the first dielectric layer and the contact; (ii) patterning the barrier layer to form the barrier structure over the contact; (iii) depositing a second dielectric layer over the patterned barrier layer and the first dielectric layer, and (iv) planarizing the second dielectric layer to expose a top surface of the barrier structure. A ferro-stack is deposited over the barrier structure. The ferro-stack includes a bottom electrode layer deposited on the barrier structure, a ferroelectric layer on the bottom electrode layer and a top electrode on the ferroelectric layer. Finally, the ferro-stack is patterned to form a ferroelectric capacitor over the barrier structure, wherein the barrier layer is conductive and a bottom electrode of the ferroelectric capacitor is electrically coupled to the contact through the barrier structure.

In one embodiment, forming the barrier structure further includes depositing a second dielectric layer over the patterned barrier layer and the top surface of the first dielectric layer, and planarizing the second dielectric layer to expose a top surface of the barrier structure.

In another embodiment, forming the barrier structure further includes encapsulating the patterned barrier layer with a hydrogen (H_2) barrier layer prior to depositing the second dielectric layer, and planarizing the second dielectric layer includes removing the H_2 barrier layer on the top surface of the barrier structure to expose the patterned barrier layer.

Optionally, patterning the barrier layer may include patterning the barrier layer to concurrently form a local interconnect (LI).

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the present invention will be understood more fully from the detailed description that follows and from the accompanying drawings and the appended claims provided below, where:

FIG. **1** (Prior Art) is a block diagram illustrating a cross-sectional views of a portion of a ferroelectric random access memory (F-RAM) cell fabricated according to a conventional method;

FIGS. **2**A and **2**B are a flowchart illustrating an embodiment of a method for fabricating a ferroelectric random access memory (F-RAM) including an embedded ferroelectric capacitor and metal-oxide-semiconductor (MOS) transistor;

FIGS. 3A-3M are block diagrams illustrating cross-sectional views of a portion of an F-RAM cell during fabrication thereof according to the method of FIGS. 2A and 2B;

FIG. 3N is a block diagram illustrating a cross-sectional views of a portion of a portion of an F-RAM cell fabricated according to the method of FIGS. 2A and 2B;

FIG. 4 is a block diagram illustrating a cross-sectional view of a portion of an F-RAM cell fabricated according to another embodiment of the method of FIGS. 2A and 2B, improve the misalignment tolerance; and

FIG. 5 is a block diagram illustrating a cross-sectional view of a portion of an F-RAM cell fabricated according to yet another embodiment of the method of FIGS. 2A and 2B.

DETAILED DESCRIPTION

Embodiments of ferroelectric random access memories (F-RAM) including embedded or integrally formed ferroelectric capacitors and complementary metal-oxide-semiconductor (CMOS) transistors and methods of fabricating the same are described herein with reference to figures. However, particular embodiments may be practiced without one or more of these specific details, or in combination with other known methods, materials, and apparatuses. In the following description, numerous specific details are set forth, such as specific materials, dimensions and processes parameters etc. to provide a thorough understanding of the present invention. In other instances, well-known semiconductor design and fabrication techniques have not been described in particular detail to avoid unnecessarily obscuring the present invention. Reference throughout this specification to "an embodiment" means that a particular feature, structure, material, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. Thus, the appearances of the phrase "in an embodiment" in various places throughout this specification are not necessarily referring to the same embodiment of the invention. Furthermore, the particular features, structures, materials, or characteristics may be combined in any suitable manner in one or more embodiments.

The terms "over," "under," "between," and "on" as used herein refer to a relative position of one layer with respect to other layers. As such, for example, one layer deposited or disposed over or under another layer may be directly in contact with the other layer or may have one or more intervening layers. Moreover, one layer deposited or disposed between layers may be directly in contact with the layers or may have one or more intervening layers. In contrast, a first layer "on" a second layer is in contact with that second layer. Additionally, the relative position of one layer with respect to other layers is provided assuming operations deposit, modify and remove films relative to a starting substrate without consideration of the absolute orientation of the substrate.

An embodiment of a method for integrating or embedding a ferroelectric capacitor into a standard or baseline CMOS process flow for fabricating an F-RAM will now be described in detail with reference to FIGS. 2A and 2B, and to FIGS. 3A-3N. FIGS. 2A and 2B are a flowchart illustrating an embodiment of a method for fabricating a ferroelectric random access memory (F-RAM) including an embedded ferroelectric capacitor and metal-oxide-semiconductor (MOS) transistor. FIGS. 3A-3M are block diagrams illustrating cross-sectional views of a portion of an F-RAM cell during fabrication thereof according to the method of FIGS. 2A and 2B. FIG. 3N is a block diagram illustrating cross-sectional views of a portion of a completed F-RAM cell including a ferroelectric capacitor fabricated according to the method of FIGS. 2A and 2B.

Referring to FIG. 2A and FIG. 3A, the process begins with planarizing surfaces of first contact plugs or contacts **302** and a first dielectric layer **304** or complementary metal-oxide-semiconductor (CMOS) layer after formation of a CMOS circuit on a surface **306** of a substrate **310**, the CMOS circuit including one or more MOS transistors **312**, separated by one or more isolation structures **314** the first dielectric layer overlying the MOS transistors and the first contacts extending through the first dielectric layer from a top surface **316** thereof to a diffusion region **318**, such as a source or a drain, of a MOS transistor in the substrate (block **202**).

In addition to a source and a drain, diffusion regions **318** can include a channel region (not shown in this figure). Generally, the substrate **310** and, hence, diffusion regions **318**, may be composed of any material suitable for semiconductor device fabrication. In one embodiment, the substrate **310** is a bulk substrate composed of a single crystal of a material which may include, but is not limited to, silicon, germanium, silicon-germanium or an III-V compound semiconductor material. In another embodiment, the substrate **310** includes a bulk layer with a top epitaxial layer. In a specific embodiment, the bulk layer is composed of a single crystal of a material which may include, but is not limited to, silicon, germanium, silicon-germanium, a III-V compound semiconductor material and quartz, while the top epitaxial layer is composed of a single crystal layer which may include, but is not limited to, silicon, germanium, silicon-germanium and a III-V compound semiconductor material. The top epitaxial layer is composed of a single crystal layer which may include, but is not limited to, silicon (i.e. to form a silicon-on-insulator (SOI) semiconductor substrate), germanium, silicon-germanium and an III-V compound semiconductor material.

The substrate **310** and, hence, the channel region, may include dopant impurity atoms. In a specific embodiment, channel region is doped P-type and, in an alternative embodiment, channel region is doped N-type. Source and drain diffusion regions **318** in the substrate **310** have opposite conductivity to channel region. For example, in one embodiment the substrate **310** and, hence, channel region, is composed of boron-doped single-crystal silicon having a boron concentration in the range of 1×10^{15}-1×10^{19} atoms/cm^3. Source and drain diffusion regions **318** are composed of phosphorous- or arsenic-doped regions having a concentration of N-type dopants in the range of 5×10^{16}-5×10^{19} atoms/cm^3. Generally, source and drain diffusion regions **318** have a depth in the substrate **310** in the range of 80-200 nanometers (nm). In accordance with an alternative embodiment of the present disclosure, source and drain diffusion regions **318** are P-type doped regions while the substrate **310** and channel region is an N-type doped region.

The MOS transistors **312** can include a gate oxide **322** formed on the surface **306** of the substrate **310**, a gate layer **324** formed on gate oxide, and one or more sidewall spacers **326** isolating the gate layer from the first dielectric layer **304**. Additionally, although not shown in this figure it will be understood by those skilled in the art that the gate layer **324** is generally electrically coupled to an overlying local interconnect (LI) or a metallization layer, such as a first metallization (MI) layer described in more detail below.

The first dielectric layer **304** can include a single layer of dielectric material or multiple layers of dielectric material as in the embodiment shown. For example, in one embodiment the first dielectric layer **304** includes a lower or bottom first dielectric layer **304a** including phosphosilicate glass (PSG) formed or deposited by a chemical vapor deposition (CVD) process, such as plasma, low pressure or atmospheric CVD, and an upper or top first dielectric layer **304***b* including a silicon oxide, deposited by low pressure CVD (LPCVD) tool using tetraethyl-orthosilicate (TEOS) based process gas or precursors.

The first contacts **302** are formed by performing a contact etch to etch the first dielectric layer **304** exposing the underlying diffusion regions **318** followed by filling the openings formed with a conductive material, typically a refractory metal. The contact etch can be accomplished using standard photolithographic techniques and any suitable wet or dry etching chemistry for etching a silicon oxide and/or PSG. Suitable contact etch chemistries can include, for example, wet etching using hydrofluoric acid (HF), or gas phase etching (GPE) using a reactive ion etch (RIE) process gas including HF and methanol or methyl alcohol (CH_3OH). Contact openings formed in the first dielectric layer **304** are filled with the refractory metal. By refractory metals it is meant metals of elements of the groups 4, 5 and 6 of the periodic table, including titanium (Ti), tantalum (Ta), tungsten (W), and nitrides or alloys thereof, which are resistant to high temperatures. The refractory metal can be deposited, for example, by physical vapor deposition, such as sputtering or evaporation, or by CVD and electroless plating.

As indicated in step or block **202** of FIG. **2**A, once formed the surfaces of the first contacts **302** and first dielectric layer **304** are planarized, for example, using a chemical mechanical polishing (CMP) process.

Next, a barrier structure (not shown in this figure) is formed over one or more of the contacts **302** over which a ferroelectric capacitor (not shown in this figure) will be formed. The barrier structure includes materials selected to form a barrier to moisture, lead, oxygen (O_2) an/or hydrogen (H_2) Referring to FIG. **2**A and FIG. **3**B forming the barrier structure begins with depositing or forming a barrier layer **328** over the planarized surfaces of the first contacts **302** and first dielectric layer **304** (block **204**). Generally, the barrier layer includes a material selected to form an O_2 barrier layer **328**. In one embodiment, not shown, the O_2 barrier layer **328** can include a single layer of a material, such as titanium-aluminum-nitride (TiAlN) having a thickness of from about 0.05 to about 0.5 μm deposited over the top surface of the first dielectric layer **304** and contacts **302**.

In other embodiments, such as that shown, the O_2 barrier layer **328** can include multiple layers including a titanium nitride (TiN) first O_2 barrier layer **328***a* having a thickness of from about 0.03 to about 0.2 μm deposited over the top surface of the first dielectric layer **304** and contacts **302**, and a titanium-aluminum-nitride (TiAlN) second O_2 barrier layer **328***b* having a thickness of from about 0.03 to about 0.10 μm deposited over the first O_2 barrier layer. Either or both of the first and second O_2 barrier layers **328** can be deposited or formed using any suitable deposition method, such as CVD, atomic layer deposition (ALD), or physical vapor deposition (PVD).

Referring to FIG. **2**A and FIG. **3**C, a mask (not shown) is formed over the O_2 barrier layer **328**, and the O_2 barrier layer **328** etched to form a patterned O_2 barrier layer **328***c* as shown in FIG. **3**C (block **206**). Generally, the patterned O_2 barrier layer **328***c* includes a number of portions that form an O_2 barrier of a number of barrier structures **330** being formed over the contacts **302**. Optionally, as in the embodiment shown, the patterned O_2 barrier layer **328***c* further includes a number of local interconnect (LI) **332** and landing pads **333**. The LI **332** electrically connect devices on top of the first dielectric layer **304**, through contacts **302** to devices formed in the CMOS or first dielectric layer, and/or devices formed above the layer on which the LI is formed through second or ferro contacts **356**, as shown in FIG. **3**N. Landing pads **333** cap some of the contacts **302** to the underlying diffusion regions **318** and serve as landing pads for additional contacts **356**, as shown in FIG. **3**N.

The mask used to form the patterned O_2 barrier layer **328***c* can include a hardmask or a photoresist mask, and the O_2 barrier layer **328** can be etched using standard photolithographic and etching techniques. For example, a TiN/TiAlN O_2 barrier layer can be dry etched using a mixture of a fluorine based gas, such as sulfur hexafluoride (SF_6), nitrogen trifluoride (NF_3) or tetrafluoromethane (CF_4), a chlorine based gas, such as chlorine (Cl_2) or Boron Trichloride (BCl_3), and, optionally, an argon gas to increase the etch rate by sputtering.

Next, referring to FIG. **2**A and FIG. **3**D forming the barrier structure further includes encapsulating the patterned O_2 barrier layer **328***c* with a hydrogen (H_2) barrier layer **334** (block **208**). It has been observed that when a ferroelectric capacitor and/or devices or transistors in the underlying CMOS circuit are exposed to hydrogen introduced, for example, during subsequent processing the properties of the ferroelectric capacitor and/or transistors in the underlying CMOS circuit can be severely degraded. In some embodiments, such as that shown, the H_2 barrier layer **334** can include multiple layers including a first hydrogen barrier layer **334***a* of aluminum oxide (Al_2O_3) having a thickness of from about 100 to about 300 Å deposited over the patterned O_2 barrier layer **328***c* by ALD, and an upper or second hydrogen barrier layer **334***b* of silicon nitride (Si_XN_Y) having a thickness of from about 0.02 to about 0.10 μm, and deposited by CVD or ALD.

Referring to FIG. **2**A and FIG. **3**E, a conformal second dielectric layer **336** is deposited over the H_2 barrier layer **334** (block **210**). Generally, as with the first dielectric layer **304**, the second dielectric layer **336** can include one or more layers of a suitable dielectric material compatible with the material of the H_2 barrier layer **334** and materials used to fabricate the ferroelectric capacitor and second contacts (not shown in this figure). Suitable dielectric material can include phosphosilicate glass (PSG) and a silicon oxide. For example, in the embodiment shown the second dielectric layer **336** includes a single layer of silicon oxide deposited by a CVD process, such as plasma, low pressure or atmospheric CVD using tetraethyl-orthosilicate (TEOS) based process gas or precursors to a sufficient for a chemical mechanical polishing (CMP) process.

Next, referring to FIG. **2**A and FIG. **3**F, the second dielectric layer **336** is polished or planarized, for example, using a CMP process to expose a top surface of the O2 barrier in the barrier structures **330** (block **212**). That is planarizing the second dielectric layer **336** comprises removing the H_2 barrier layer **334** on a top surface of the barrier structure **330** to expose the second O_2 barrier layer **328***b*. It will be understood that as in the embodiment shown, in those embodiments in which patterning O_2 barrier layer **328** (block **206**) further includes patterning O_2 barrier layer to form a number of local interconnect (LI) **332** planarizing the second dielectric layer **336** may also include removing the H_2 barrier layer(s) **334** on a top surface of the LI **332** to expose the second O_2 barrier layer **328***b*.

Referring to FIG. **2**A and FIG. **3**G layers of a ferro stack from which a ferroelectric capacitor will be formed are deposited or formed over the planarized surfaces of the second dielectric layer **336**, the preformed or pre-patterned, barrier structures **330** and the LI **332** (block **214**). Generally, the ferro stack layers includes a layer of a ferroelectric material, such as a lead zirconate titanate (PZT) ferroelectric layer **338**, between a top electrode **340** and bottom electrode **342** in electrical contact with or electrically coupled to one of the underlying first contacts **302** through the electrically conductive material of the O_2 barrier **328** of the barrier structure **330**, and through the contact to the diffusion region **318** of the MOS transistor **312**.

The top and the bottom electrodes **340**, **342**, can include one or more layers of iridium or iridium oxide having a thickness of from about 0.05 to about 0.20 μm, and deposited or formed using CVD, ALD or PVD. In the embodiment shown the top electrode **340** is a multi-layer top electrode including, for example, a lower layer of iridium oxide (IrO2) in contact with the PZT ferroelectric layer **338** and an upper layer of iridium (Ir) overlying the lower layer of the top electrode. The PZT ferroelectric layer **338** is deposited on the bottom electrode **342** to a thickness of from about 0.04 to about 0.10 μm, using CVD, ALD or PVD.

Referring to FIG. **2**A and FIG. **3**H a patterned hardmask **344** is formed over the ferro-stack layers **338**, **340**, **342**, using standard photolithographic and etching technologies (block **216**). In certain embodiments, the hardmask **344** can include multiple layers and the material of the hardmask is selected to form a barrier, such as a hydrogen (H_2) barrier, that is left on the ferro-stack layers after etching to form a ferroelectric capacitor (not shown). The hardmask **344** can include, for example, a layer of titanium aluminum nitride (TiAlN) having a thickness of from about 0.15 to about 0.20 μm, and deposited or formed using a PVD process. Suitable chemistries and techniques for etching the hardmask **344** can include using a mixture of a fluorine based gas, such as sulfur hexafluoride (SF_6), nitrogen trifluoride (NF_3) or tetrafluoromethane (CF_4), a chlorine based gas, such as chlorine (Cl_2) or Boron Trichloride (BCl_3), and, optionally, an argon gas to increase the etch rate by sputtering.

Next, referring to FIG. **2**A and FIG. **3**I the ferro stack layers **338**, **340**, **342**, are patterned using the patterned hardmask **344** and standard etching technologies to form a ferroelectric capacitor **346** over the previously fabricated barrier structure **330** (block **218**). Suitable chemistries and techniques for etching the ferro stack layers can include standard metal etch chemistries, including for example, high density plasma (HDP) etching, and various post-metal etch cleaning processes to prevent corrosion defects. It will be understood that a significant advantage of the method of the present disclosure is that because the ferroelectric capacitor **346** is formed over the pre-patterned barrier structure **330** is that conductive residues formed during etching or patterning of layers to form the barrier structure, are not re-deposited on sidewalls of the ferroelectric capacitor, as would happen if the barrier structure **330** were formed after etching of the ferro stack layers **338**, **340**, **342**. Conductive residues on sidewalls of the ferroelectric capacitor **346** forming a high leakage path between bottom electrode **342** and top electrode **340** impairing operation of the ferroelectric capacitor, or, when the conductive residues are excessive, shorting the bottom electrode and top electrode rendering the ferroelectric capacitor completely inoperative.

Referring to FIG. **2**B and FIG. **3**J, a second H_2 barrier or H_2 encapsulation layer **348** is deposited over a top and sidewalls of the ferroelectric capacitor **346** and over the surface the LI **332**, any exposed surface of the second dielectric layer **336**, substantially encapsulating the ferroelectric capacitor (block **220**). It has been observed that when the ferroelectric capacitor **346** is exposed to hydrogen introduced, for example during subsequent processing, the properties of the ferroelectric capacitor can be severely degraded. The second H_2 encapsulation layer **348** can include a single material layer, or multiple material layers. In one embodiment, such as that shown, second H_2 encapsulation layer **348** can include a lower or first hydrogen encapsulation layer **348***a* of aluminum oxide (Al_2O_3) having a thickness of from about 100 to about 300 Å, and deposited by ALD, and an upper or second hydrogen encapsulation layer **348***b* of silicon nitride (Si_xN_y), having a thickness of from about 0.02 to about 0.10 μm, and deposited by CVD or ALD.

Referring to FIG. **2**B and FIG. **3**K, a third dielectric layer **350** or ILD is deposited or formed over the H_2 encapsulation layer **348** and planarized (block **222**). The third dielectric layer **350** can include one or more layers of an undoped oxide, such as silicon-dioxide (SiO_2), a nitride, such as silicon nitride (Si_xN_y), a silicon-oxynitride ($Si_xO_yN_z$) or, as with the first dielectric layer **304** described above an oxide, such as phosphosilicate glass (PSG). For example, in one embodiment the third dielectric layer **350** can include a SiO_2 having a final, post CMP thickness of from about 0.1 to about 0.3 μm from the top of the H_2 encapsulation layer **348**, by deposited by LPCVD using TEOS.

Next, referring to FIG. **2**B and FIG. **3**L a patterned mask layer **352** is formed on the third dielectric layer **350** (block **224**), and, referring to FIG. **2**B and FIG. **3**M openings **354** are etched through third dielectric layer **350** for ferro or second contacts (not shown) to electrically couple, through the hardmask **344**, to the top electrode **340** of the ferroelectric capacitor **346**, and to LI **332** using standard photolithographic and etching technologies (block **226**). For an SiO_2 third dielectric layer **350** suitable masking and etching techniques can include forming a patterned photoresist layer, and etching the third dielectric layer with an etch chemistry comprising carbon-monoxide (CO), argon (Ar), octafluorocyclobutane (C_4F_8) or Freon® 318, and, optionally, nitrogen (N_2).

Referring to FIG. **2**B and FIG. **3**N, a ferro contact openings **354** are filled to form second or ferro contacts **356** (block **228**). As with the first contacts **302** described above, the ferro contacts **356** are formed by filling the contact openings with a refractory metal, such as titanium (Ti), tantalum (Ta), tungsten (W), and nitrides or alloys thereof, by physical vapor deposition, such as sputtering, evaporation or CVD. After filling the second contact openings the contacts **356** and third dielectric layer **350** are planarized using, for example, a CMP process. FIG. **3**N is a block diagram illustrating a cross-sectional view of a substantially completed portion of an F-RAM cell including a ferroelectric capacitor **346**, and fabricated according to the method of FIGS. **2**A and **2**B.

Next, referring to FIG. **2**B and again to FIG. **3**N a metal layer is deposited over the third dielectric layer **350** and masked and etched to form a first metallization (Ml) layer **358** (block **230**). Generally, the metal layer can be or include aluminum, copper or alloys or mixtures thereof, and is deposited by PVD, such as sputtering, evaporation, or electroless plating to a thickness of from about 1000 to about 5000 Å. The metal layer is patterned to form the Ml layer **358** using standard photolithographic and metal etching techniques, including for example, high density plasma (HDP) etching, and various post-metal etch cleaning processes to prevent corrosion defects.

It will be understood by those skilled in the art that the embodiment of a method of manufacturing or fabricating an F-RAM cell including embedded or integrally formed ferroelectric capacitor and CMOS transistors described above advantageously minimizes changes to the standard complimentary metal-oxide-semiconductor (CMOS) process flow, including the addition of just two additional mask steps, thereby reducing cost of fabricating ferroelectric random access memories (F-RAM).

It will be further understood that a number of layers in the completed ferroelectric capacitor **346** is reduced by at least one layer, i.e., a O_2 barrier that is typically formed and patterned with the ferro stack layers formed in a conventional method, and a stack height of the ferroelectric capacitor is reduced by about 30% over, those formed by the conventional method. In addition, the challenge of etching the ferro stack layers **338**, **340**, **342** is reduced due to the change in aspect ratio, enabling the sidewalls of the ferroelectric capacitor **346** to be more vertical, and providing a larger cap size (top surface of the ferroelectric capacitor) for the same design layout. In addition to the above, the thinner third dielectric layer **350** enables a lower aspect ratio for the second or ferro contacts **356**, facilitating contact etch and fill, and increasing a yield of working devices. Finally, it is noted that by forming the LI **332** and landing pads **333** from the patterned O_2 barrier layer **328***c* substantially eliminates the potential for oxidizing metal used in the underlying first contacts **302** during subsequent processing.

FIG. **4** is a block diagram illustrating a cross-sectional view of a portion of a completed F-RAM fabricated according to an alternate embodiment of the method of FIGS. **2**A-**2**B and **3**A-N. Referring to FIG. **4**, in this embodiment the patterning the ferro-stack to form the ferroelectric capacitor **346** over the previously fabricated barrier structure **330**, block **218**, comprises patterning the ferro-stack to form a bottom electrode **342** having a larger area in a plane parallel to the surface **306** of the substrate **310** than an area of the barrier structure **330**. It will be understood by those skilled in the art that this embodiment wherein the barrier structure **330** has a smaller dimension compared to bottom electrode **342** of the ferroelectric capacitor **346** will improve the misalignment tolerance, thereby facilitating the fabrication processes and increasing a yield of the working devices.

FIG. **5** is a block diagram illustrating a cross-sectional view of a portion of a completed F-RAM fabricated according to another alternate embodiment of the method of FIGS. **2**A-**2**B and **3**A-N. Referring to FIG. **5**, in this embodiment the hydrogen barrier layer(s) **334***a*, **334***b*, are omitted or replaced by the substitution of a silicon nitride (Si_3N_4) layer **360** for the SiO_2 of the second dielectric layer **336**. Silicon nitride layer **360** can be deposited by CVD or ALD over patterned O_2 barrier layer **328***c* (shown in FIG. **3**C) and planarized, for example, using a CMP process such as that described in relation to block **212** in relation to FIGS. **3**E and **3**F.

Thus, embodiments of ferroelectric random access memories including embedded or integrally formed F-RAM capacitors and CMOS transistors and methods of fabricating the same have been described. Although the present disclosure has been described with reference to specific exemplary embodiments, it will be evident that various modifications and changes may be made to these embodiments without departing from the broader spirit and scope of the disclosure. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

The Abstract of the Disclosure is provided to comply with 37 C.F.R. §1.72(b), requiring an abstract that will allow the reader to quickly ascertain the nature of one or more embodiments of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims. In addition, in the foregoing Detailed Description, it can be seen that various features are grouped together in a single embodiment for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as reflecting an intention that the claimed embodiments require more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive subject matter lies in less than all features of a single disclosed embodiment. Thus, the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate embodiment.

Reference in the description to one embodiment or an embodiment means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the circuit or method. The appearances of the phrase one embodiment in various places in the specification do not necessarily all refer to the same embodiment.

What is claimed is:

1. A method comprising:

forming a contact extending through a first dielectric layer on a surface of a substrate;

forming a barrier structure over the contact, wherein forming the barrier structure comprises, depositing a barrier layer over the first dielectric layer and the contact, patterning the barrier layer to form the barrier structure over the contact, and depositing a second dielectric layer over the patterned barrier layer and the first dielectric layer, and planarizing the second dielectric layer to expose a top surface of the barrier structure;

depositing a ferro-stack over the barrier structure, the ferro-stack including a bottom electrode layer deposited on the barrier structure and second dielectric layer, a ferroelectric layer on the bottom electrode layer and a top electrode on the ferroelectric layer; and

patterning the ferro-stack to form a ferroelectric capacitor over the barrier structure, wherein the barrier layer is conductive and a bottom electrode of the ferroelectric capacitor is electrically coupled to the contact through the barrier structure.

2. The method of claim **1**, wherein the barrier layer comprises a material selected to form an oxygen (O_2) barrier layer.

3. The method of claim **2**, wherein the O_2 barrier layer comprises multiple layers including a titanium nitride first O_2 barrier layer deposited over the top surface of the first dielectric layer and the contact, and a titanium-aluminum-nitride (TiAlN) second O_2 barrier layer deposited over the first O_2 barrier layer.

4. The method of claim **2**, wherein forming the barrier structure further comprises encapsulating the patterned O_2 barrier layer with a hydrogen (H_2) barrier layer prior to depositing the second dielectric layer over the patterned O_2 barrier layer, and wherein planarizing the second dielectric layer comprises removing the H_2 barrier layer on the top surface of the barrier structure to expose the patterned O_2 barrier layer.

5. The method of claim **4**, wherein the H_2 barrier layer comprises multiple layers including an aluminum oxide (Al_2O3) layer deposited over the patterned O_2 barrier layer, and a silicon nitride layer over the Al_2O_3 layer.

6. The method of claim **4**, wherein patterning the barrier layer comprises patterning the barrier layer to concurrently form a local interconnect (LI), and wherein encapsulating the patterned O_2 barrier layer comprises encapsulating the LI with the H_2 barrier layer.

7. The method of claim **6**, wherein planarizing the second dielectric layer to expose the top surface of the barrier structure further comprises concurrently removing the H_2 barrier layer on a top surface of the LI.

8. The method of claim **1**, wherein patterning the ferro-stack to form the ferroelectric capacitor over the barrier structure, comprises patterning the ferro-stack to form a bottom electrode having a larger area than the barrier structure.

9. The method of claim 1, wherein the barrier structure comprises material selected to form a barrier to moisture, lead, O_2 or H_2.

10. The method of claim 1, wherein forming a contact extending through a first dielectric layer comprises forming a contact to a diffusion region of a metal-oxide-semiconductor (MOS) transistor in the surface of the substrate.

11. A method comprising:

forming a contact extending through a first dielectric layer on a surface of a substrate;

forming a barrier structure over the contact, wherein forming the barrier structure comprises: (i) depositing a barrier layer over a top surface of the first dielectric layer and the contact; (ii) patterning the barrier layer to form the barrier structure over the contact and to concurrently form a local interconnect (LI); and (iii) depositing a second dielectric layer over the patterned barrier layer and the first dielectric layer, and planarizing the second dielectric layer to expose top surfaces of the barrier structure and LI;

depositing a ferro-stack over the barrier structure, the ferro-stack including a bottom electrode layer deposited on the barrier structure, a ferroelectric layer on the bottom electrode layer and a top electrode on the ferroelectric layer; and

patterning the ferro-stack to form a ferroelectric capacitor over the barrier structure, wherein the barrier layer is conductive and a bottom electrode of the ferroelectric capacitor is electrically coupled to the contact through the barrier structure.

12. The method of claim 11, wherein the barrier layer comprises a material selected to form an oxygen (O_2) barrier layer.

13. The method of claim 12, wherein the O_2 barrier layer comprises multiple layers including a titanium nitride first O_2 barrier layer deposited over the top surface of the first dielectric layer and the contact, and a titanium-aluminum-nitride (TiAlN) second O_2 barrier layer deposited over the first O_2 barrier layer.

14. The method of claim 12, wherein forming the barrier structure further comprises encapsulating the patterned O_2 barrier layer with a hydrogen (H_2) barrier layer prior to depositing the second dielectric layer over the patterned O_2 barrier layer, and wherein planarizing the second dielectric layer comprises removing the H_2 barrier layer on top surfaces of the barrier structure and LI.

15. The method of claim 14, wherein the H_2 barrier layer comprises multiple layers including an aluminum oxide (Al_2O3) layer deposited over the patterned O_2 barrier layer, and a silicon nitride layer over the Al_2O_3 layer.

16. The method of claim 11, wherein forming a contact extending through a first dielectric layer comprises forming a contact to a diffusion region of a metal-oxide-semiconductor (MOS) transistor in the surface of the substrate.

17. A method comprising:

forming a contact extending through a first dielectric layer on a surface of a substrate to a diffusion region of a metal-oxide-semiconductor (MOS) transistor formed in the surface of the substrate;

depositing an oxygen (O_2) barrier layer over the top surface of the first dielectric layer and the contact;

patterning the O_2 barrier layer to form a barrier structure over the contact;

encapsulating the patterned O_2 barrier layer with a hydrogen (H_2) barrier layer;

depositing a second dielectric layer over the patterned H_2 barrier layer and the first dielectric layer;

planarizing the second dielectric layer to remove the H_2 barrier layer on a top surface of the barrier structure to expose the patterned O_2 barrier layer;

depositing a ferro-stack over the barrier structure, the ferro-stack including a bottom electrode layer deposited on the barrier structure, a ferroelectric layer on the bottom electrode layer and a top electrode on the ferroelectric layer; and

patterning the ferro-stack to form a ferroelectric capacitor over the barrier structure, wherein the barrier layer is conductive and a bottom electrode of the ferroelectric capacitor is electrically coupled to the contact through the barrier structure.

18. The method of claim 17, wherein patterning the O_2 barrier layer comprises patterning the O_2 barrier layer to concurrently form a local interconnect (LI), and wherein encapsulating the patterned O_2 barrier layer comprises encapsulating the LI with the H_2 barrier layer.

19. The method of claim 18, wherein planarizing the second dielectric layer to expose the top surface of the barrier structure comprises concurrently removing the H_2 barrier layer on a top surface of the LI.

20. The method of claim 19, wherein the O_2 barrier layer comprises multiple layers including a titanium nitride first O_2 barrier layer deposited over the first dielectric layer and the contact, and a titanium-aluminum-nitride (TiAlN) second O_2 barrier layer deposited over the first O_2 barrier layer, and the H_2 barrier layer comprises multiple layers including an aluminum oxide (Al_2O3) layer deposited over the patterned O_2 barrier layer, and a silicon nitride layer over the Al_2O_3 layer.

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